QUAD CMOS-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

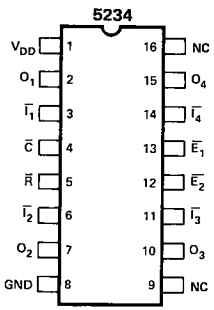
- **CMOS Technology for Very Low Power: Suitable for Battery Backup**
- **High Density: Four Drivers in One Package**
- **Internal Gating Structure Minimizes Package Count**
- **CMOS Compatible Inputs**
- **CerDIP Package: 16 Pin DIP**
- **Only One Power Supply Required, +12V (±10%)**

The Intel® 5234 is a Quad CMOS-to-MOS driver which accepts CMOS input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107A or 2107B. The circuit operates from a single 12 volt power supply.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system design.

The Intel ion-implanted, silicon gate, Complementary MOS (CMOS) process allows the design and production of very low power drivers.

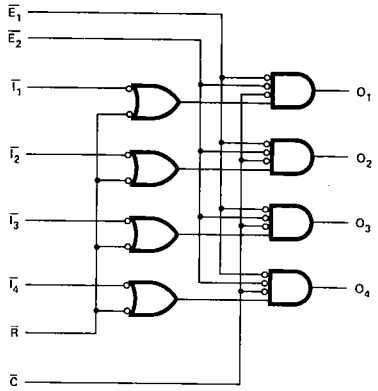
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	$\overline{C}$	CLOCK CONTROL INPUT
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
		NC	NOT CONNECTED

LOGIC DIAGRAM



Final Data Sheet Information Will Be Available In Second Quarter 1976.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -0.5 to (V_{DD}+0.5V)
Outputs for Clock Driver . . . . . -0.5 to (V_{DD}+0.5V)
Power Dissipation at 25°C 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = 12V ±10%.

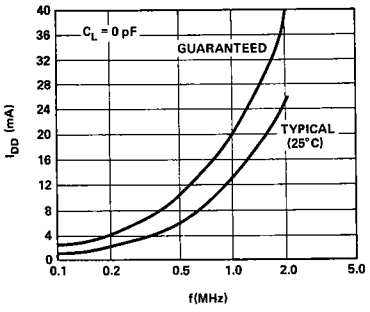
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Load Current			0.1	μA	V_{IN} = 0 to V_{DD}
V_{OL}	Output Low Voltage		0.15	0.4	V	I_{OL} = 5mA
		-1.0	-0.15			I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.4	V_{DD}-0.15		V	I_{OH} = -5mA
			V_{DD}+.15	V_{DD}+0.5		I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs			2.0	V	
V_{IH}	Input High Voltage, All Inputs	V_{DD}-2.0			V	
I_{DD}	Supply Current		0.1	100	μA	V_{DD} = 13.2V, f = 0
I_{DD1}	Supply Current		13	20	mA	V_{DD} = 13.2V, f = 1MHz, C_L = 0, (See Figure 1)

Note 1: Typical values are at 25°C and nominal voltage.

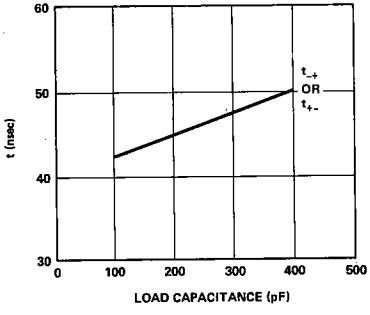
Typical Characteristics

FIGURE 1

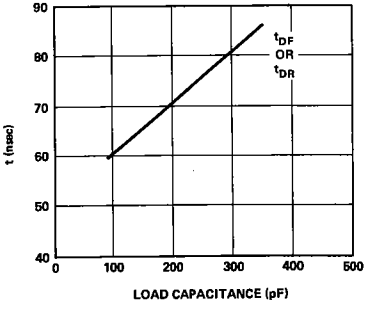
POWER SUPPLY CURRENT VS. FREQUENCY (ALL 4 CHANNELS SWITCHING)



INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE



DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE



MEMORY SUPPORT

A.C. Characteristics $T_A = 0°$ to $70°C$, $V_{DD} = 12V \pm 10\%$.

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit
t_{-+}	Input to Output Delay	20	45		ns
t_{DR}	Delay Plus Rise Time		70	100	ns
t_{+-}	Input to Output Delay	20	45		ns
t_{DF}	Delay Plus Fall Time		70	100	ns
t_T	Output Transition Time	10	25	40	ns

NOTES: 1. $C_L = 150pF$
2. $C_L = 200pF$
3. $C_L = 250pF$

These values represent a range of total stray plus clock capacitance for nine 4K RAMs.

4. Typical values are measured at 25°C.

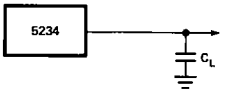
Capacitance* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	8	14	pF

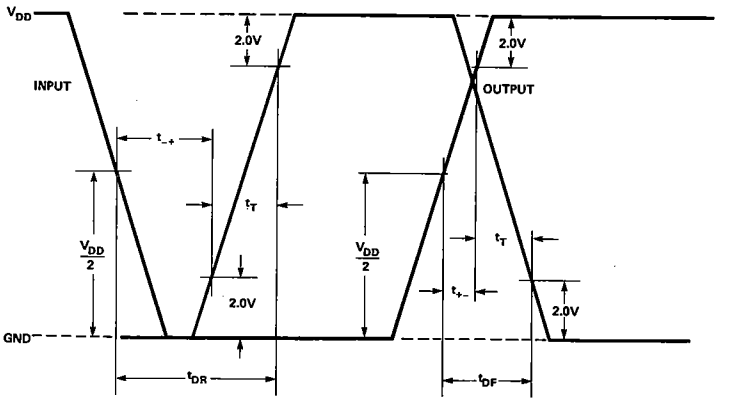
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 0 to V_{DD}
Input Pulse Rise and Fall Times: 40 ns between 10% and 90% points
Measurement Points: See Waveforms



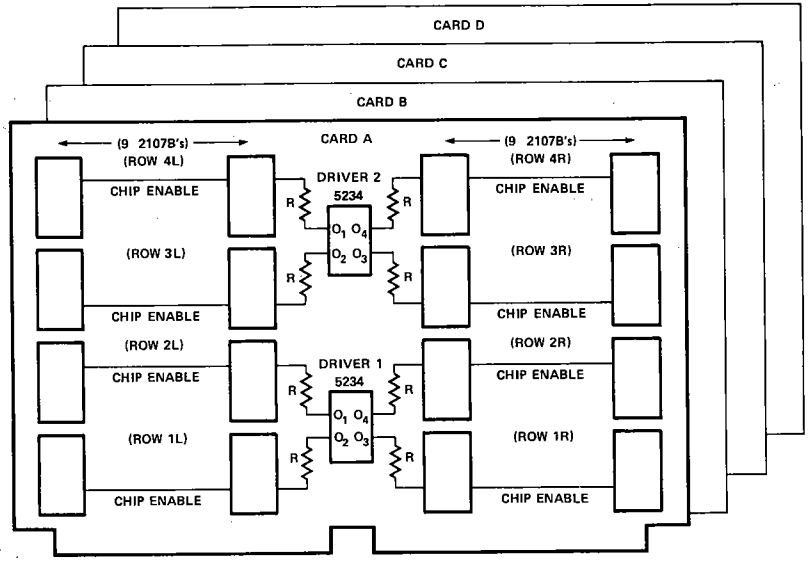
Waveforms



MEMORY SUPPORT

Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 5234 quad high voltage driver for the chip enable inputs. A single 5234 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



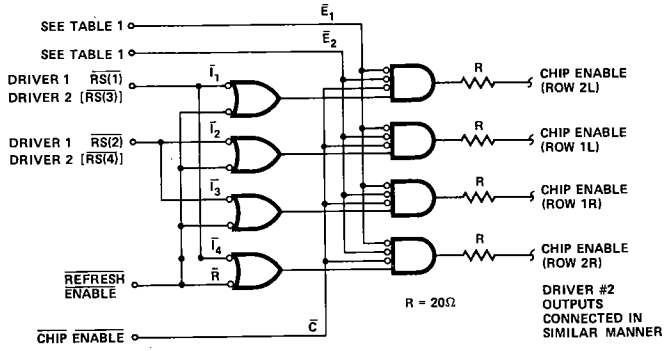


TABLE 1.

CARD	INPUTS $\bar{E}_1$	INPUTS $\bar{E}_2$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
C	ENABLE N	ENABLE P
D	ENABLE N	ENABLE Q